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H4R RLS
U1S S2206

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GB 2249002 A GB 2244160 A GB 2030740 A

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INT CL[5] H04N 5/04

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(54) Signal synchroniser with resynchronise control

(57) A video/audio signal synchroniser with a circular memory buffer has the facility to resynchronise its output by adjusting the relative positions of its read and write pointers at a desired arbitrary time so that a minimum period in which the output is free of resynchronisation disturbance can be guaranteed to follow. The operation is carried out automatically, when either input or reference signals are connected, or manually, by pressing a switch or providing an input signal to the synchroniser from external equipment.

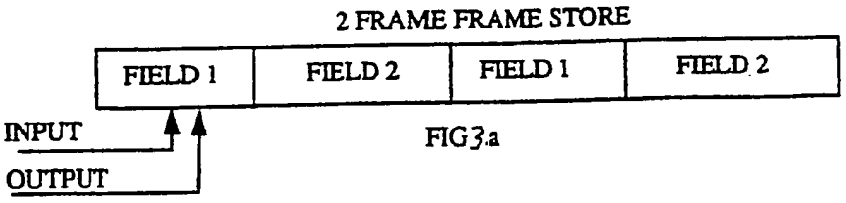

FIG3a

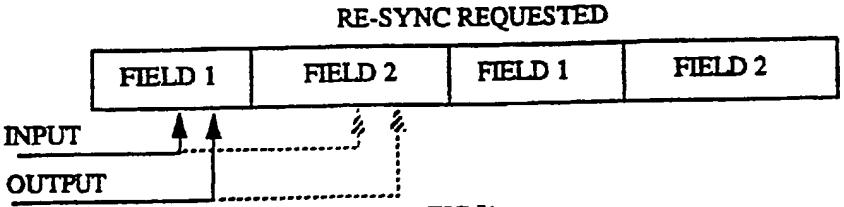

FIG 3b

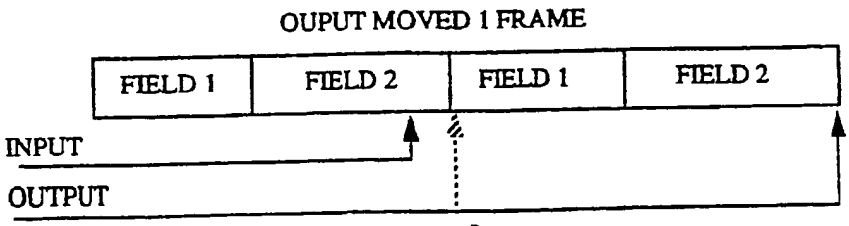

FIG3c

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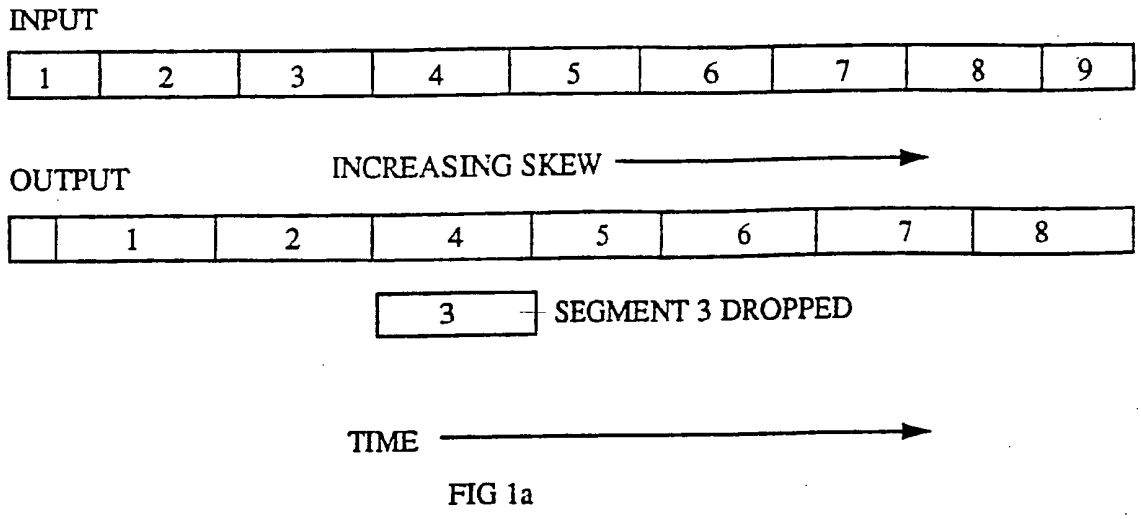

INPUT
1
2
3
4
5
6
7
8
9
OUTPUT
INCREASING SKEW
1
2
4
5
6
7
8
3
SEGMENT 3 DROPPED
TIME

FIG 1a

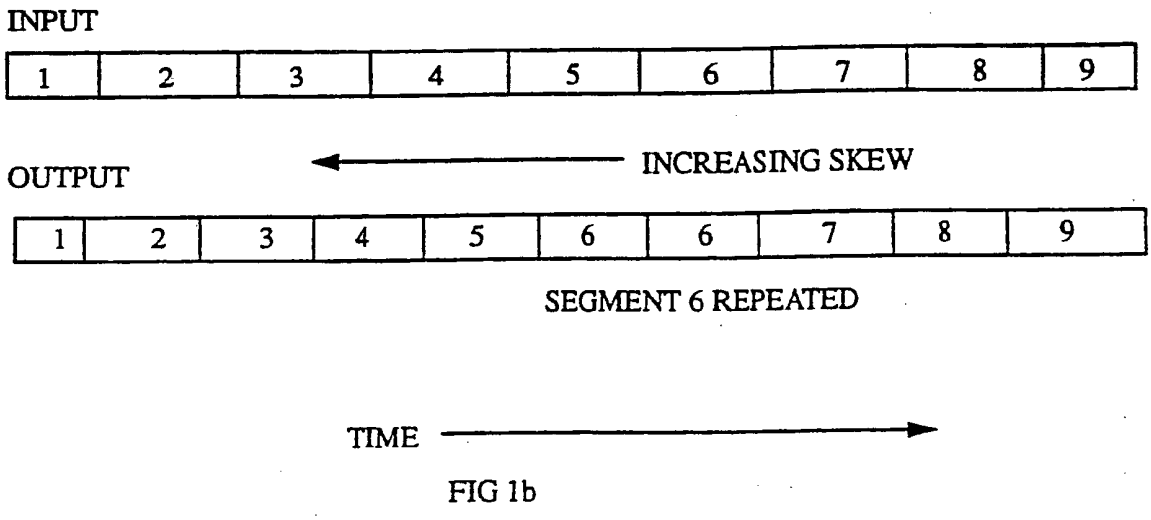

INPUT
1
2
3
4
5
6
7
8
9
OUTPUT
INCREASING SKEW
1
2
3
4
5
6
6
7
8
9
SEGMENT 6 REPEATED
TIME

FIG 1b

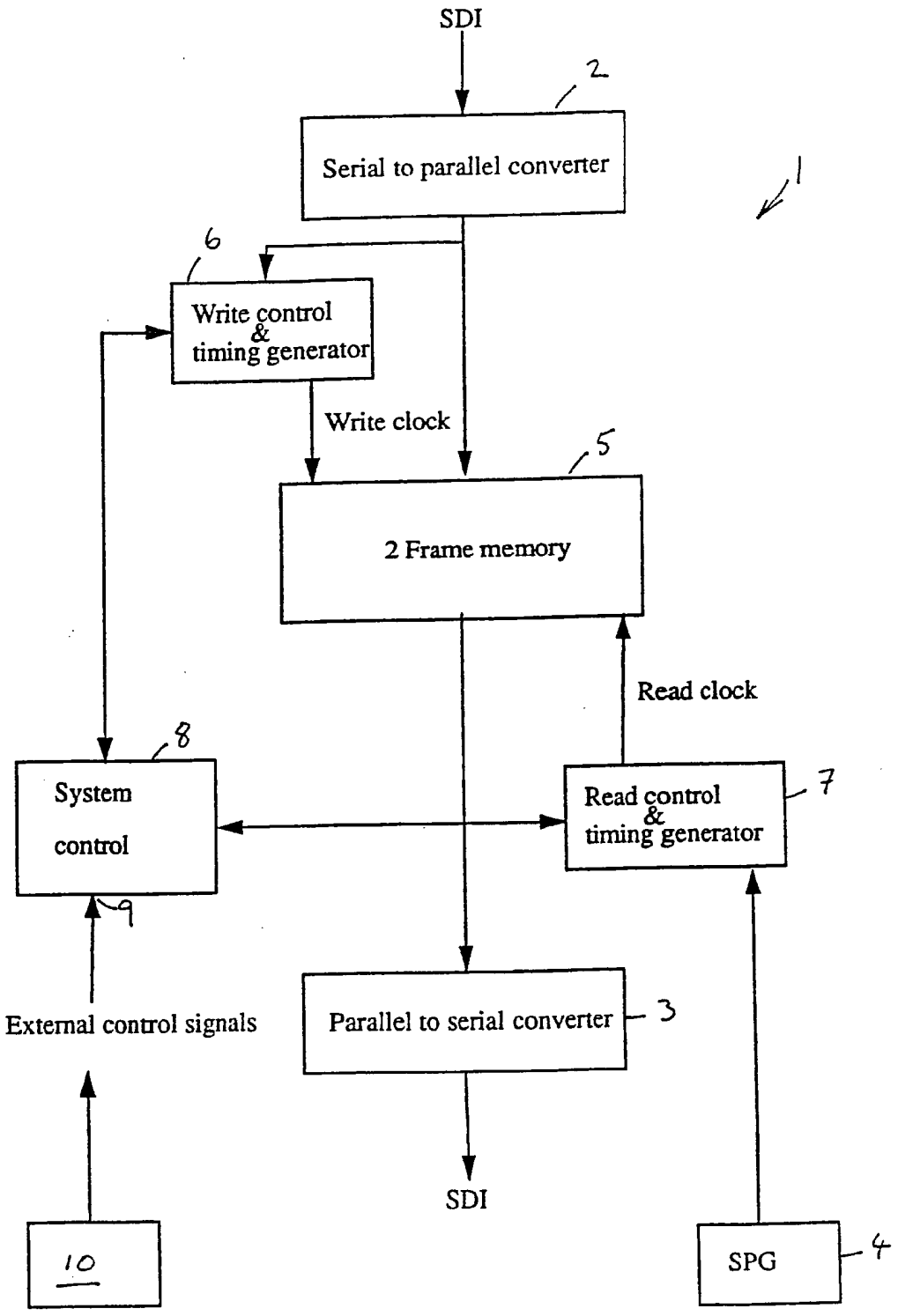

SDI
2
Serial to parallel converter
1
6
Write control & timing generator
Write clock
5
2 Frame memory
Read clock
8
System control
7
Read control & timing generator
9
External control signals
Parallel to serial converter
3
SDI
10
SPG
4

FIG 2

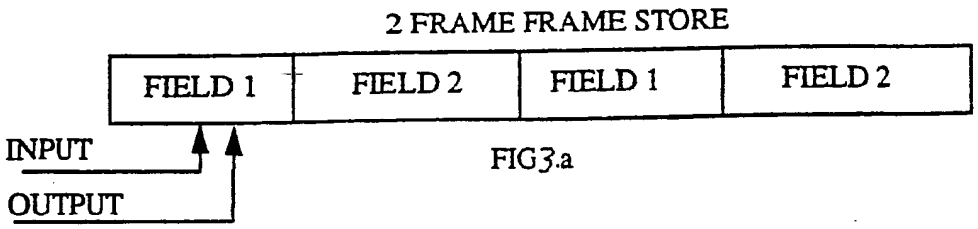


FIG3.a

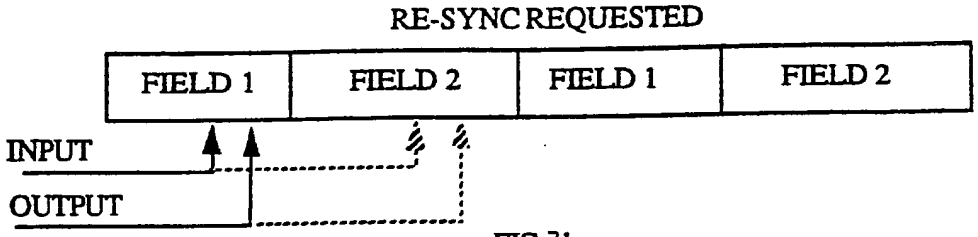


FIG 3b

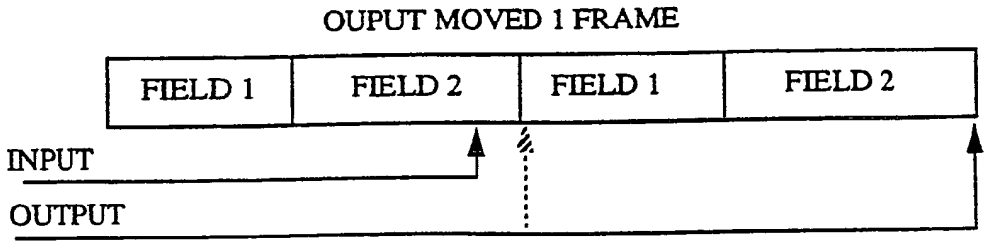


FIG3c

SIGNAL SYNCHRONISER WITH RESYNCHRONISE CONTROL

The present invention relates to a signal synchroniser, in particular a synchroniser for video/audio signals.

When video programme material is assembled, e.g. for recording or broadcasting, from independent sources which do not share a common clock signal, it is necessary to synchronise the source signal with a reference signal which may be derived from either a master reference source or one of the other sources. This is done by passing the source signal through a synchroniser.

Although video signals operating to the same video standards are nominally of the same frequency, unless they are clocked from the same master reference (which is often impractical) they will have an arbitrary phase relationship which is subject to continual change; in those circumstances a synchroniser is typically used to fix the phase of the signals outputted from it relative to some reference. The synchroniser essentially consists of a circular or ring-buffer into which the signal is written at a rate determined by the source and from which the signal is read at a rate determined by the destination. The locations at which the signal data is written and read are determined by write- and read-pointers to addresses within the buffer.

The amount of slippage of phase which the synchroniser can accommodate between its input and output depends on the capacity of its memory buffer. A progressive drift of phase in one direction or the other would eventually cause the buffer to overflow or underflow. In order to avoid this, it is necessary to monitor for the onset of these conditions and to preempt a possible overflow or underflow by causing the read pointer to jump over addresses of the buffer memory. This necessarily results in the stored information being dropped or repeated to ensure

that synchronisation is maintained.

In the accompanying drawings, Figures 1a and 1b illustrate the skew which arises from phase slippage between the input and output of the synchroniser.

Due to the stability of sync pulse generators (SPGs) used with sources of video signals, the disturbance brought about by the necessary jumping of the synchroniser read pointer actually occurs very infrequently.

For example, the colour sub-carrier-frequency for the 625/50Hz colour television signal is specified to be 4.43361875 MHz ± 1Hz, and all horizontal and vertical timing information can be derived from this sub-carrier. Synchronising (sync.) pulse generators (SPGs) are designed to meet and are generally better than this specification.

Given the ± 1Hz tolerance, this approximates to a 1 part in 4 million error. There are 88600 cycles of sub-carrier in one 60Hz field, so it will therefore take 88600/3600 = 24.628 hours for this 1 part in 4 million error to cause a "jump" in the synchroniser output.

In the worst case condition, one reference may be + 1Hz whilst the other reference is - 1Hz. This represents a 2 part in 4 million error which reduces the above time to 12.31 hours.

With current synchronisers, it is impossible to predict the point in time when this disturbance will occur. The frame disturbance could therefore occur instantaneously, or after twelve hours, or some point in between.

It would be desirable to ensure that this disturbance did not occur whilst the program was actually on air (being transmitted) or recorded.

As will be apparent from the above the interval between "jumps" in the synchroniser output depends on the rate of phase slippage between the input and output (which is determined by the SPGs used) and the capacity of the synchroniser memory. However, it would be impractical to

attempt to reduce the rate of phase slippage (the input to the synchroniser might be from an external source over which no timing control could be exercised) and increasing the capacity of the memory buffer would increase its cost. In any event, since it must be assumed that the relative phasing of the input and output of the signal cannot be guaranteed, there is no practical way to predict when a jump in synchroniser output will occur.

The present invention is based upon an appreciation of the fact that despite the above, a synchroniser can be operated in such a way as to guarantee that a jump in output will not occur within a given interval of time, so allowing the recording or broadcast to proceed within that interval. The invention achieves this by providing the facility to request resynchronisation of the output of the synchroniser at any desired, arbitrary time, so that it can be known that a jump in the output of the synchroniser will not occur at least for a minimum interval after that; this is done by adjusting the relative positions of the write and read pointers by adjusting the read and/or write addresses. Thus, according to the present invention there is provided a video signal synchroniser comprising:-

a) a circular memory buffer for storing video data and having a capacity of at least two frames of video data;

b) means for writing successive incoming video data into the memory buffer at a series of locations determined by a write pointer whose position is successively changed in synchronism with the incoming video data;

c) means for reading data stored in the memory buffer at locations by a read pointer whose position is successively changed at a rate synchronised with a read clock unsynchronised with the incoming video data and for delivering the read-out data to an output; and

d) means, responsive to a signal which is

produced at any arbitrary desired time and which designates a request to resynchronise the output of the synchroniser video data, to adjust the relative positions of teh read and write pointers to increase the separations in both directions around the buffer between the write and read pointers provided the current read and write pointer positions and the capacity of the buffer, permit it.

Resynchronisation of the synchroniser output may be requested by an externally generated signal or by removal or reconnection of the input signal or the synchronisation signal. Resynchronisation is essentially an initialisation operation and essentially involves determining whether the read and/or write pointers can be repositioned in such a way as to increase the separation (in the forward and reverse directions around the buffer) between the write and read pointers preferably while maintaining continuity of the output of the synchroniser, and, if so, moving the read and/or write pointers accordingly. Suitable logic within the synchroniser can make the necessary determinations. It is preferable that the jump in the read pointer address actually occurs between frames. Accordingly the logic within the synchroniser may be arranged so that if a request for resynchronisation is received part way through a frame, that request is flagged as pending until the end of the current, or a later frame whereupon it is processed and acted upon.

In order to preserve continuity of the output of the synchroniser across a resynchronisation operation, during the jump the read pointer should be moved by an integral multiple of one frame of video data. Using a jump of an integral number of frames preserves the odd/even/odd sequence of fields outputted from the synchroniser.

This optimisation or "re-synchronisation" feature can be carried out automatically when either input or reference signals are connected, or manually by pressing a

switch or providing an input signal to the synchroniser from external equipment.

Applying this feature causes the frame jump re-alignment of sources to occur at a known time, the synchroniser operation should then be transparent for a minimum period.

Assuming the synchroniser has an internal store of two video frames, it can be guaranteed that the "re-synchronisation" feature will always be able to optimise the input and output separation to one field minimum.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings, in which:-

Figures 1a and 1b illustrate the effect of correcting phase skew in a synchroniser;

Figure 2 illustrates in block form an implementation of the illustrated embodiment of the present invention; and

Figures 3a to 3c illustrate stages in the resynchronisation operation of an embodiment of the invention.

Figure 2 illustrates, in block diagram form, one embodiment of synchroniser 1 in accordance with the present invention. The synchroniser 1 is provided with a so-called Serial Digital Interface that handles incoming and outgoing video/audio signals as a bit-serial stream. In such a stream, the audio data accompanying the video material is digitised, and time-base compressed into blocks interleaved between the video samples at the horizontal and vertical intervals of the video signal. The resulting signal is at 270 Mbits per second with a ten bits per sample.

The incoming video/audio data which has a frequency and phase determined by its source is converted from serial to 10-bit parallel form by a serial/parallel converter 2.

The output from synchroniser 1, delivered via parallel to serial converter 3 is a corresponding series of digital video/audio data which is synchronised in frequency and phase with a local signal pulse generator 4 running independently of that of the incoming data; the SPG 4 may be a local master timing source or may derive its synchronisation from another source of timing signals, e.g. another local video source.

Internally, the synchroniser 1 includes a memory buffer 5 having a capacity of two or more whole frames' worth of the video/audio data. The incoming data is written into it at an address determined by a write pointer WP and the outgoing data is read from an address determined by read pointer RP. The write and read pointer values WP,RP are generated by a pair of counters within write and read control and timing circuits 6 and 7 which are clocked by respective clock signals. The write clock and timing signals are derived from the serial data from serial to parallel converter 2 from the incoming data; the read clock and timing signals are derived from SPG 4. The counters within write and read control and timing circuits 6 and 7 are arranged to wrap around between values corresponding to low and high addresses of the memory 5 so that the memory 5 operates as a circular buffer as described above.

A system control circuit 8 associated with the write and read control and timing circuits 6 and 7 receives the current write- and read-pointer values and derives timing signals from them; it comprises resynchronisation logic which operates to implement the resynchronisation feature of the invention by responding to an externally generated signal received at input 9 representing a request for resynchronisation from a source such as a user operable push switch 10. An indicator device (not shown) may be provided to indicate that the resynchronisation request has been acted upon and may if desired, give a display or other

indication of the time remaining of the guaranteed minimum jump free period following the resynchronisation. This period may be calculated by the system controller 8 from measured or assumed values for the maximum rates of drift of the clock sources. A calculation based on assumed values may be implemented very simply by loading a counter within system controller 8 with a suitable value when a resynchronisation operation occurs and decrementing it at periodic intervals thereafter.

In order to process a resynchronisation request, the system controller 8 operates as follows:-

1) When a resynchronisation request is received at input 9, the request is flagged as pending e.g. by setting a hardware latch or software variable. No further action is taken until the end of the current frame of the output signal.

2) Each time the system controller 8 detects that the read pointer address has reached a value corresponding to the end of a frame, it determines whether a resynchronisation request is pending. If not, no further action is taken, otherwise it proceeds to the next step.

3) The system controller 8 evaluates the current values of the read and write pointers and determines whether the separation, in the forward and reverse directions around the buffer, can be increased given the overall size of the buffer by repositioning the read pointer at the end of the other frame of data. If it can, it sends a signal to the read control and timing circuit 7 to reposition the read pointer accordingly. Note: where the buffer has a capacity of more than two frames, the resynchronisation logic circuit can select which of the frames other than the current one will maximise the separation between the read and write pointers.

4) The system controller 8 clears the resynchronisation request flag and updates the indicator

(if provided).

Figure 3a shows a condition of the synchroniser 1 where the write pointer position is very close to the read pointer position, i.e. less than one field.

At some time later (Figure 3b), "re-synchronisation" is requested, as by operation of the push-switch 10.

At the next output frame boundary, the output data pointer RP is moved to the end of the next frame (Figure 3c). This is the same as dropping a segment of data as shown in Figure 1a. The separation between input and output is now greater than one frame in one direction and just less than one frame in the other direction.

Depending on the direction of drift of the phase between input and output, the synchroniser will now be stable for greater than 12 hours or just less than 12 hours, given the 1 part in 4 million stability of the SPGs and the worst case situation mentioned above of one clock being 1Hz over the chrominance subcarrier frequency and the other by 1Hz under.

If the input and output are already separated by more than one field when "re-synchronisation" is requested, then with a two frame storage capacity, the separation cannot be improved, unless the direction of drift of the changing phase relationship can be predicted and of course that the direction of drift can be guaranteed not to change.

If a larger store were provided in the synchroniser, then more scope for input output separation could also be provided, thus allowing a greater time of transparent operation to be guaranteed.

Thus the present invention can provide a way of providing a guaranteed period of transparent operation of a video/audio synchroniser.

The "re-synchronisation" feature can be automatically or manually invoked.

A synchroniser having this feature will always optimise the input and output separation to give the largest period possible of disturbance free operation, given the limitations of memory buffer storage size and reference signal stability.

If either the input or output reference signals are removed for any reason, then the synchroniser can automatically implement this feature.

An external input signal could also be used to provide optimised input/output separation. This could be used for instance at the start of day's transmission or recording to provide the maximum disturbance free operation possible.

CLAIMS

1. A video signal synchroniser comprising:-

a) a circular memory buffer for storing video data and having a capacity of at least two frames of video data;

b) means for writing successive incoming video data into the memory buffer at a series of locations determined by a write pointer whose position is successively changed in synchronism with the incoming video data;

c) means for reading data stored in the memory buffer at locations by a read pointer whose position is successively changed at a rate synchronised with a read clock unsynchronised with the incoming video data and for delivering the read-out data to an output; and

d) means, responsive to a signal which is produced at any arbitrary desired time and which designates a request to resynchronise the output of the synchroniser video data, to adjust the relative positions of teh read and write pointers to increase the separations in both directions around the buffer between the write and read pointers provided the current read and write pointer positions and the capacity of the buffer, permit it.

2. A synchroniser according to claim 1, wherein the means, d) to adjust the relative positions of the read and write pointers is operative to move their relative positions by an integral multiple of one frame of data.

3. A synchroniser according to claim 1 or 2, wherein the capacity of the memory buffer is two frames of data and the means, d) to adjust the relative positions of teh read and write pointers is operative to move the read pointer from the data of one frame to the position of corresponding data in the other.

4. A synchroniser according to claims 1, 2 or 3, wherein the means, d) is operative to adjust the read pointer and/or write pointers when the read pointer reaches the data at the end of the frame currently being read.

5. A synchroniser according to any one of the preceding claims and adapted for operation with a video signal of a format in which samples of audio data associated with video material are interleaved in the horizontal and vertical periods between samples of video data.

6. A synchroniser according to any one of the preceding lcaims and including means for indicating that a resynchronisation request has been acted upon.

7. A synchroniser according to any one of the preceding claims wherein indicating means are provided to indicate the time remaining of the minimum jump free period following synchronisation.

8. A synchroniser constructed and arranged to operate substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

12 | Application number: GB 9304588.8

Relevant Technical fields

(i) UK Cl (Edition L) H4P (PSFX, PSX, PT, PV); H4R (RLS); G4A (AFT, AKBI)

(ii) Int Cl (Edition 5) H04N 5/04

Search Examiner: K WILLIAMS

Date of Search: 7 JUNE 1993

Databases (see over)

(i) UK Patent Office

(ii)

Documents considered relevant following a search in respect of claims 1 TO 7

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	GB 2249002 A (GPT) see pages 2 to 5	1
A	GB 2244160 A (BBC) see Abstract and Figure 2	1
A	GB 2030740 A (MARCONI) see Abstract and EP 0012497 A2	1

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

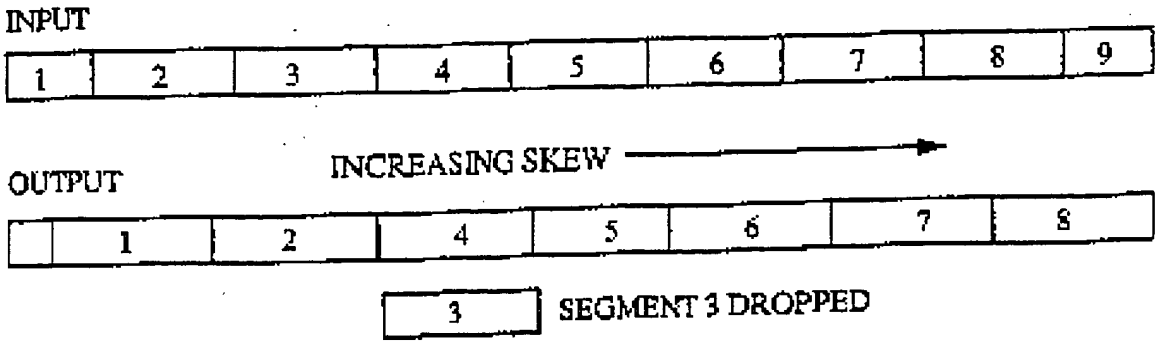
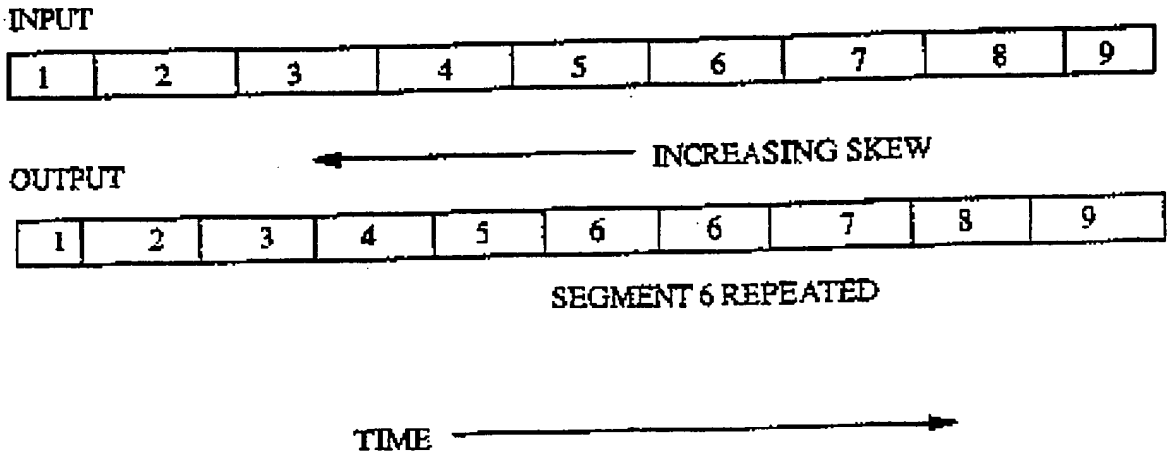

INPUT
1
2
3
4
5
6
7
8
9
OUTPUT
INCREASING SKEW
1
2
4
5
6
7
8
3
SEGMENT 3 DROPPED
TIME

FIG 1a


INPUT
1
2
3
4
5
6
7
8
9
INCREASING SKEW
OUTPUT
1
2
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6
7
8
9
SEGMENT 6 REPEATED
TIME

FIG 1b

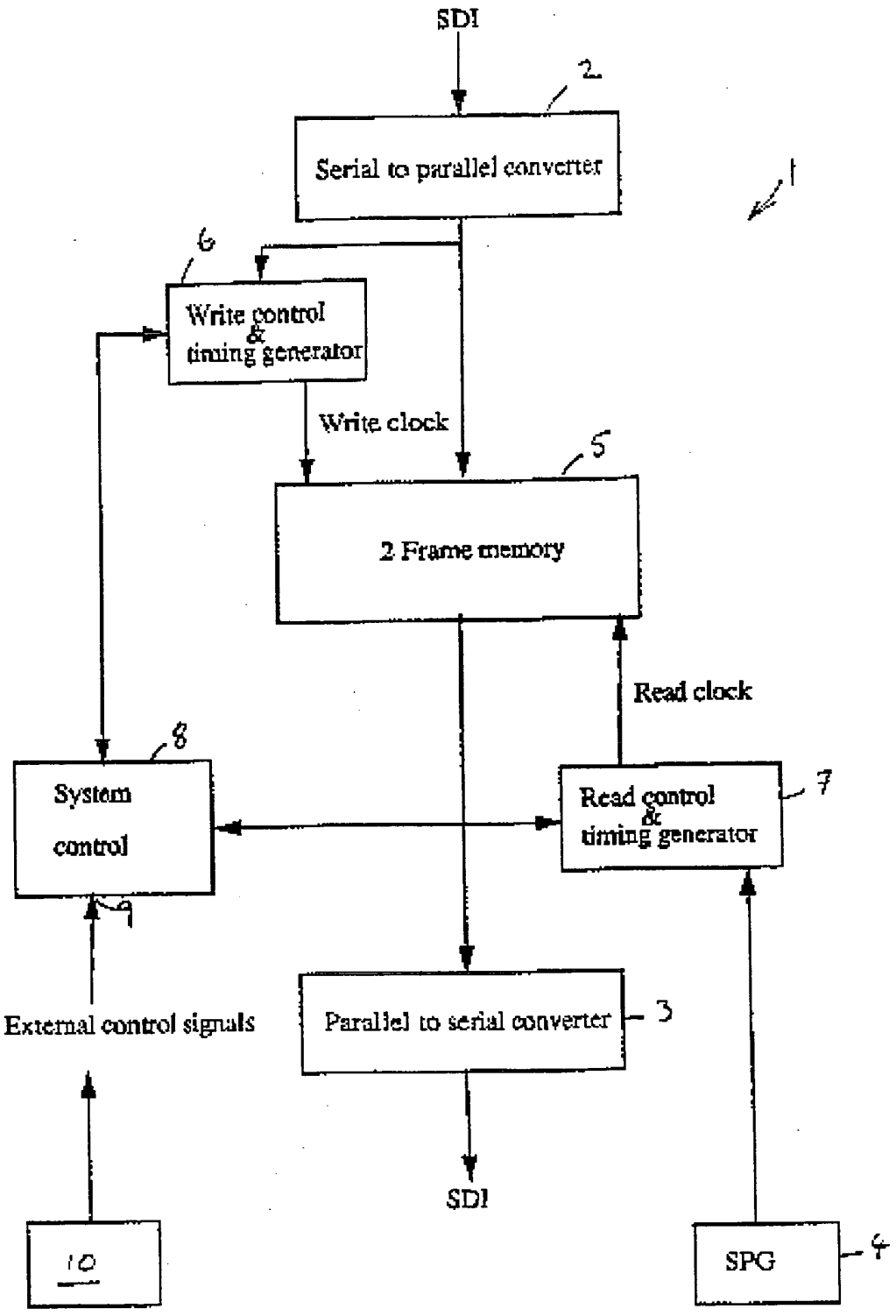
SDI
2
Serial to parallel converter
1
6
Write control & timing generator
Write clock
5
2 Frame memory
Read clock
8
System control
7
Read control & timing generator
9
External control signals
Parallel to serial converter
3
SDI
10
SPG
4

FIG 2

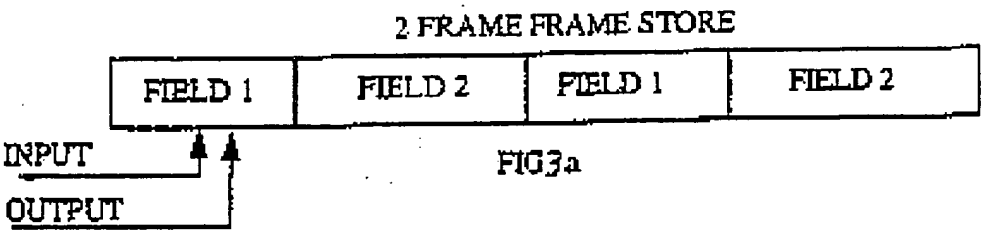

FIG3a

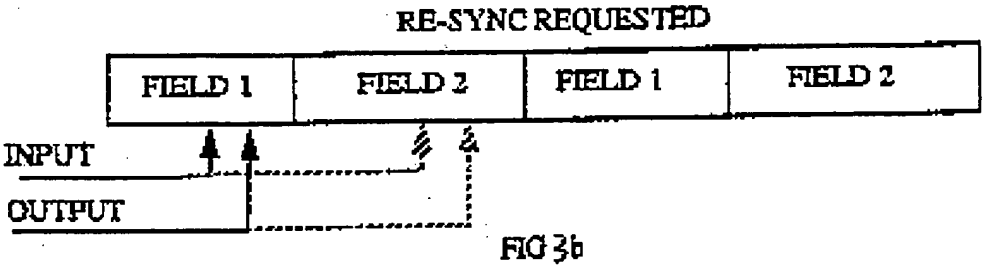

FIG 3b

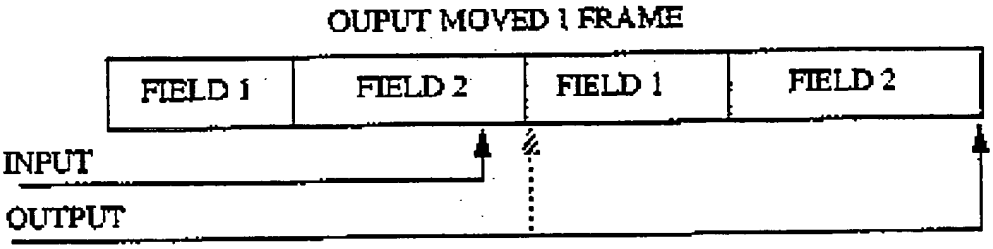

FIG 3c